wherein a first width of said well isolation structure between said first and second device regions is smaller than a second width of said well isolation structure between said third and fourth device regions.

17. (New) The semiconductor device according to claim 16, wherein said first, second, third and fourth device regions have substantially same configuration.

18. (New) A semiconductor device comprising:

a first well of p type and a second well of n type disposed adjacent to each other;

a well isolation structure comprising a shallow trench formed on a boundary of said first and second wells;

a pair of a first device region of n type and a second device region of p type, said first and second device regions being disposed to oppose each other, with said well isolation structure disposed between said first device region and said second device region;

a third device region of n type and fourth device region of p type, said third and fourth device regions being disposed not to oppose each other, with said well isolation structure disposed between said third device region and said fourth device region;

wherein said first and third device regions are provided in said first well and said third and fourth device regions are provided in said second well, and a first width of said well isolation structure between said first and second device regions is smaller than a second width of said well isolation structure between said third and fourth device regions.

REMARKS

The office action of May 22, 2002 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 8 and 16-18 are pending. Claim 1 has been canceled without prejudice or disclaimer and new claims 16-18 have been added. Claims 2-7 and 9-15 have been canceled without prejudice or disclaimer as being drawn to non-elected invention(s).

Claims 1 and 8 stand objected to for informalities and/or defects. These informalities have been addressed in the amendment to claim 8 and in new claims 16-18. Withdrawal of this objection is requested.

Claim 8 stands rejected under 35 U.S.C. § 112, first paragraph, as being based on a disclosure which is not enabling. Claim 8 has been amended and new claims 16 and 18 have been added to recite semiconductor devices fully enabled by the specification. Withdrawal of this rejection is requested.

Claims 1 and 8 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 1 has been canceled, new independent claims 16 and 18 added, and claim 8 has been amended, to clarify the invention. Withdrawal of this rejection is requested.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,252,280 (Hirano). Claim 1 has been canceled and new claims 16-18 have been added. Insofar as the instant rejection applies to new claims 16-18, it is respectfully in error.

The instant claims require two sets (pairs) of device regions (active areas), which are disposed in two wells adjacent to each other with a well isolation structure disposed between each set of device regions. Hirona merely discloses a single set (pair) of device regions and thus does not teach two sets of device regions in accordance with claims 16-18. Hirano does not teach each and every element of the claimed invention as required under 35 USC 102 and withdrawal of the instant rejection is requested.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hirano in view of U.S. patent no. 6,091,630 (Chan et al.) Hirano does not teach or suggest the claimed invention for the reasons described above for independent claim 16. Chan does not teach or suggest two sets of device regions in accordance with claim 16. Thus, Chan does not remedy the defects of Hirano. Withdrawal of the instant rejection is requested.

CONCLUSION

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: October 22, 2002

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MARKED-UP VERSION OF AMENDMENTS MADE

IN THE SPECIFICATION:

Page 2, lines 4-7:

In case of Fig. ~~8~~9A, an n^+ diffusion layer 15, which is a device region, is formed on the surface part of the p-well 13, but no device region exists in the opposite position in the n-well side. This is called an open space.

Page 2, line 36 to page 3, line 7:

Figs. 12A and 12B show results of an experiment in actual formation of devices. Fig. 11A shows those of devices in which device regions are not opposed whereas Fig. ~~11~~12B shows those of devices in which device regions are opposed. This result shows that, in devices where device regions are not opposed, the withstand voltage property decreases to an unusable level when the STI width reaches 0.2 μm, but in devices where device regions are opposed, they maintains a sufficient withstand voltage even under 0.2 μm.

Page 4, lines 6-9:

forming a first well of a first conductivity and ~~and~~ a second well of a second conductivity which is opposite to the first conductivity in a manner they are disposed adjacent to each other;

Page 6, lines 20-30:

As shown in Fig. 4, device regions 15 and 16 are partly opposed, but since their opposed extensions are not sufficiently wide, tapered angle does not increase sufficiently, and well isolation distance cannot be reduced sufficiently. To compensate it, a p^+ dummy region 19 is formed to extend from one side of the p^+ region 16 such that the n^+ region 15 is opposed with its full width. As a result, similarly to the configuration of Fig. 1, there exists a pattern of opposed device regions, and miniaturization of devices can be attained by using more miniaturized well isolation.

MARKED-UP VERSION OF AMENDMENTS MADE

Page 6, line 32 to page 7, line 4:

If the concept of Embodiment 2 is used, opposed device regions need not be those actually used. That is, they may be dummy device regions. Fig. 5 shows an example of this concept, and a dummy pattern 20 is formed to confront the n^+ region 15. Note, however, that its width has to completely include the portion opposed to the width of the n^+ region 15. Therefore, if the dummy region has the width equal to the width of the n^+ region 15 as illustrated with the solid line, or a wider width as illustrated with the broken line, the requirement is satisfied.

Page 9, lines 5-14:

After that, 5 nm thick SiO_2 is formed on the Si substrate by thermal oxidation of 800EC, and an ion implantation pattern is formed by photo lithography. There follows ion implantation of arsenic to n^+ regions under the acceleration voltage of 35 KeV by the dose of $2x10^{14}cm^{-2}$, and ion implantation of BF_2 to p^+ regions under the acceleration voltage of 10 KeV by the dose of $2x10^{14}cm^{-2}$. Subsequently, by annealing at 1000EC for 30 seconds in N_2 atmosphere, a shallow n^+ layer ~~114~~113 is formed in the p-well 108 and a shallow p^+ layer 114 is formed in the n-well (Fig. 8G).

IN THE CLAIMS:

Claim 8 has been amended as follows:

8. (Amended) The semiconductor device according to claim ~~1~~16, wherein ~~opposed~~ said device regions act as ~~are cell patterns of~~ static RAM cells~~, and a well isolation structure having a narrower width than other circuit blocks is used~~.